

## Claims

[c1] A method of forming CMOS semiconductor materials with a PFET area and an NFET area formed on a semiconductor substrate, said PFET area being covered with a PFET gate dielectric layer and said NFET area covered with an NFET gate dielectric layer composed of silicon oxide with different degrees of nitridation thereof, providing a silicon substrate with a PFET area and an NFET area, forming a PFET gate oxide layers over said PFET area and an NFET gate oxide layer over said NFET area, providing nitridation of said PFET gate oxide layer above said PFET area to form said PFET gate dielectric layer above said PFET area with a first concentration level of nitrogen atoms in said PFET gate dielectric layer above said PFET area, providing nitridation of said NFET gate oxide layer to form said NFET gate dielectric layer above said NFET area, whereby an NFET concentration level of nitrogen atoms in said NFET gate dielectric layer is different from a PFET concentration level of nitrogen atoms in said PFET gate dielectric layer.

- [c2] The method of claim 1 including performing the following steps with one thereof preceding the other:  
forming an NFET mask over said NFET area prior to beginning nitridation of said PFET gate oxide layer, then performing PFET gate dielectric nitridation thereof, and immediately thereafter removing said NFET mask, and forming a PFET mask over said PFET area prior to beginning nitridation of said NFET gate oxide layer, then performing NFET gate dielectric nitridation thereof, and immediately thereafter removing said PFET mask.
- [c3] The method of claim 1 including performing the following steps with one thereof preceding the other:  
forming a single mask over one of said NFET area and said PFET area prior to beginning nitridation leaving the other of said regions as an unmasked region, performing gate dielectric nitridation of said unmasked region, and immediately thereafter removing said single mask, and performing gate dielectric nitridation into both said NFET area and said PFET area adding an equal concentration of nitrogen to said NFET gate oxide layer and said PFET gate oxide layer.
- [c4] The method of claim 1 including performing the following steps with one thereof preceding the other:  
forming a capacitor dielectric mask over said NFET area and said PFET area prior to beginning nitridation of a ca-

pacitor dielectric layer in a capacitor region, then performing capacitor dielectric nitridation thereof, and immediately thereafter removing said capacitor dielectric mask, and

forming an FET mask over a previously formed capacitor region prior to beginning nitridation of said gate oxide layer in said NFET area and said PFET area, then performing FET gate dielectric nitridation thereof, and immediately thereafter removing said FET mask.

[c5] The method of claim 1 including providing greater nitridation in said PFET gate dielectric layer above said PFET area than nitridation in said NFET gate dielectric layer above said NFET area.

[c6] The method of claim 2 including providing greater nitridation in said PFET gate dielectric layer above said PFET area than nitridation in said NFET gate dielectric layer above said NFET area.

[c7] The method of claim 3 including providing greater nitridation in said PFET gate dielectric layer above said PFET area than nitridation in said NFET gate dielectric layer above said NFET area.

[c8] The method of claim 4 including providing greater nitridation in said PFET gate dielectric layer above said PFET

area than nitridation in said NFET gate dielectric layer above said NFET area.

[c9] A method of forming CMOS semiconductor materials with a PFET area and an NFET area formed on a semiconductor substrate, said PFET area being covered with a PFET gate dielectric layer and said NFET area covered with an NFET gate dielectric layer composed of silicon oxide and different degrees of nitridation thereof, providing a silicon substrate with a PFET area and an NFET area, forming a PFET gate oxide layer over said PFET area and an NFET gate oxide layer over said NFET area, providing nitridation of said PFET gate oxide layer above said PFET area to form said PFET gate dielectric layer above said PFET area with a first concentration level of nitrogen atoms in said PFET gate dielectric layer above said PFET area, providing nitridation of said NFET gate oxide layer to form said NFET gate dielectric layer above said NFET area, whereby an NFET concentration level of nitrogen atoms in said NFET gate dielectric layer is less than said first concentration level of nitrogen atoms in said PFET gate dielectric layer, and said NFET gate dielectric layer and said PFET gate dielectric layer have the same thickness.

[c10] The method of claim 9 including performing the following steps with one thereof preceding the other:  
forming an NFET mask over said NFET area prior to beginning nitridation of said PFET gate oxide layer, then performing PFET gate dielectric nitridation thereof, and immediately thereafter removing said NFET mask, and forming a PFET mask over said PFET area prior to beginning nitridation of said NFET gate oxide layer, then performing NFET gate dielectric nitridation thereof, and immediately thereafter removing said PFET mask, forming a single mask over one of said NFET area and said PFET area prior to beginning nitridation leaving the other of said regions as an unmasked region, performing gate dielectric nitridation of said unmasked region, and immediately thereafter removing said single mask, and performing gate dielectric nitridation into both said NFET area and said PFET area adding an equal concentration of nitrogen to said NFET gate oxide layer and said PFET gate oxide layer, with a resulting total nitrogen content higher in said PFET gate oxide layer.

[c11] The method of claim 9 including performing the following steps with one thereof preceding the other:  
forming a capacitor dielectric mask over said NFET area and said PFET area capacitor dielectric region prior to beginning nitridation of a capacitor dielectric layer in a

capacitor dielectric region, then performing capacitor dielectric nitridation thereof, and immediately thereafter removing said capacitor dielectric mask, and forming an FET mask over said a capacitor dielectric region prior to beginning said nitridation of said gate oxide layer in NFET area and said gate oxide layer in said PFET area, then performing FET gate dielectric nitridation thereof, and immediately thereafter removing said FET mask.

- [c12] The method of claim 9 including providing greater nitridation in said PFET gate dielectric layer above said PFET area than nitridation in said NFET gate dielectric layer above said NFET area.
- [c13] The method of claim 1 wherein the nitridation process is performed at a temperature below the maximum temperature that the masking material can withstand.
- [c14] The method of claim 2 wherein the nitridation process is performed at a temperature below the maximum temperature that the masking material can withstand.
- [c15] The method of claim 3 wherein the nitridation process is performed at a temperature below the maximum temperature that the masking material can withstand.
- [c16] The method of claim 4 wherein the nitridation process is

performed at a temperature below the maximum temperature that the masking material can withstand.

[c17] The method of claim 5 wherein the nitridation process is performed at a temperature below the melting maximum temperature that the masking material can withstand.

[c18] The method of claim 6 wherein the nitridation process is performed at a temperature below the maximum temperature that the masking material can withstand.

[c19] The method of claim 7 wherein the nitridation process is performed at a temperature below the maximum temperature that the masking material can withstand.

[c20] A CMOS semiconductor device with a PFET area and an NFET area formed on a semiconductor substrate, said PFET area being covered with a PFET gate dielectric layer and said NFET area covered with an NFET gate dielectric layer composed of silicon oxide and different degrees of nitridation thereof comprising:

a silicon substrate with said PFET area and said NFET area,

a PFET gate dielectric layer over said PFET area and an NFET gate dielectric layer over said NFET area,

said PFET gate dielectric layer and said NFET gate dielectric layer having different levels of nitridation whereby a

PFET concentration level of nitrogen atoms in said PFET gate dielectric layer above said PFET area is different from the an NFET concentration level of nitrogen atoms in said NFET gate dielectric layer.